S.E - IV Sem - Biomed. 6/6/16

06/2016 Logic Circuits (21) St/IV/CBGS/Bm/LC

QP Code:534600

(3 Hours) [Total Marks :80

N.B. : (1) Question No. 1 is compulsory.
(2) Attempt any 3 out of remaining 5 questions
(3) Figures to the right indicates full marks.
(4) Assume suitable data wherever it is necessary.

1. Solve any four:- 20
   (a) Design half adder using NOR gates
   (b) Derive characteristic equation of JK F/F
   (c) State and prove De-Morgan's theorem.
   (d) What are reflective codes?
   (f) Convert JK F/F to D Flip Flop.

2. (a) Design synchronous mod 4 Up/Down counter using JK F/F 10
   (b) Draw and explain 2i/p TTL NAND gate. What are salient features of TTL family 10

3. (a) Design Gray($G_3G_2G_1G_0$) to Binary ($B_3B_2B_1B_0$) Converter 10
   (b) What is a race around condition in SR F/F 5
   (c) Design 32:1 multiplexer using two 16:1 multiplexers. 5

4. (a) Design a 2 bit multiplier (A_1A_0) with (B_1B_0) 10
   (b) Explain why NAND and NOR gates are called universal gates? 2
   (c) Design following gates:- 8
      (i) EX-OR using NAND
      (ii) EX-NOR using NOR

5. (a) Explain operation of 1:4 demultiplexer 5
   (b) Prove $BC + A\overline{C} + AB + BCD = BC + A\overline{C}$ 5
   (c) Design a BCD to seven segment decoder for common cathode using logic circuits 10

6. Write short notes on any four:- 20
   (a) Bidirectional shift register
   (b) Hazards in combinational circuits
   (c) Counter ICs
   (d) Positive and Negative edge triggering
   (e) Design a 3 bit even parity generater

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