S.E- IV Sem- Biomed

Logic Circuits.

(24) QP Code : 5491

(3 Hours) [Totai Marks : 80

N.B. : (1) Question no 1 is compulsory
(2) Attempt any three remaining 5 questions.
(3) Figures to the right indicate full marks.
(4) Assume suitable data wherever it is necessary.

1. Solve any four 20
(a) State and prove De-Morgan's theorem
(b) Show that

$$A\overline{B}C + B + B\overline{D} + AB\overline{D} + \overline{A}C = B + C$$

(c) What is shaft position encoding?
(d) Explain weighted codes
(e) Explain with respect to Flip-flop
(i) Level triggering
(ii) Edge triggering

2. (a) Design a 2 bit magnitude comparator Compare ($A_1 A_0$) with ($B_1 B_0$) 10
(b) Explain the operation of SR Flip-flops using NAND gates. What is a race around condition. 10

3. (a) Design Gray ($G_3 G_2 G_1 G_0$) to binary ($B_3 B_2 B_1 B_0$) Converter 10
(b) Design 32 :1 Multiplexer using two 16:1 multiplexers. 5
(c) Derive characteristics equation of SR Flip-flop. 5

4. (a) Design the following gates 8
(i) NOR using NAND
(ii) NAND using NOR
(b) Design a 2 bit multiplier 7
($A_1 A_0$ with $B_1 B_0$)
(c) Explain bidirectional shift register 5

5. (a) Explain 2 input TTL NAND gate along with diagram. 10
(b) Design Synchronous Mon- 4 up-down counter using J K FlipFlop. 10

6. Write short notes on **any four** 20
(a) Counter IC's
(b) Quine Mcclusky's technique
(c) Debounce switch
(d) Half subractor using NAND gates
(e) 5 & 6 Variable K maps.

MD-Con. 11586-15.