SE/Biomed/Rev/IV/KT. 15/12/14

(1) Logic Circuits (20)

QP Code :12558

(3 Hours) **[Total Marks : 80**

N.B. : (1) Attempt any **four** questions from **six** questions.
(2) **Figures** to the **right** indicate **full** marks.
(3) Assume **suitable** data wherever is **required.**

1. Solve short notes on (any **four** :– **20**
   (a) Hazards in combinational circuits
   (b) De-Morgans theorem
   (c) RAM and ROM
   (d) Debounce switch
   (e) Weighted codes.

2. (a) Design a 2 bit (A_1 A_0) with (B_1 B_0) multiplier. Implement it using gates. **10**
   (b) Differentiate between combinational and sequential logic circuits. **5**
   (c) Derive characteristic equation of SR Flip Flop. **5**

3. (a) Reduce the following function using Quine Mccluskey method. **10**
   $f(A, B, C, D) = \Sigma m(0, 1, 4, 5, 6, 7, 9, 10, 15) + d(11, 14)$
   (b) Implement the following function using :– **10**
      (i) Only one 8:1 Multiplexer
      (ii) Only one 4:1 Multiplexer and gates
      $f(A, B, C, D) = \Sigma m(1, 2, 3, 7, 10, 11)$.

4. (a) Design a MOD–10 synchronous counter using JK Flip Flop. Draw transition table, kmaps and state transition diagram. Do not let unused states return to zero. **10**
   (b) Explain positive and negative edge triggering. **5**
   (c) Show that – **5**

$$A\overline{B}C + B + B\overline{D} \div A\overline{B}\overline{D} + \overline{A}C = B + C.$$

5. (a) Convert the following data into Hamming code – **5**
      (i) 1101 (ii) 1000.
   (b) Explain two input TTL NAND gate along with diagram. **10**
   (c) What is shaft position encoding. **5**

6. Write short notes on (any **four**) :– **20**
   (a) Explain bidirectional shift register
   (b) Design 3 bit Gray (G_2 G_1 G_0) to Binary (B_2 B_1 B_0) converter.
   (c) What are standard and non standard SOP and POS forms ?
   (d) Explain five and six variabe K maps
   (e) Design 3 bit odd parity generator
   (f) Design half subtractor using NAND gates.

****

GN-Con.:11510-14.