S.E/Biomed./SemIV/Choice Based/Digital Electronics

29/5/18

Digital electronics

Q.P. Code : 21325

(19)

[Time: 3 Hours] [Marks: 80]

Please check whether you have got the right question paper.

N.B:
1. Question **No. 1** is **compulsory**.
2. Attempt any **Three** questions from remaining Five questions.
3. Answers should be supported by diagrams, waveforms and theorems if any.

Q.1 Solve any five questions out of six questions.

(a) Design a combinational logic circuit to count the number of 1's in a 3 bit data. 04

(b) State and prove De-Morgan's theorems. 04

(c) State the steps involved is Quine McClusky's method. 04

(d) Implement 4:1 MUX using logic gates. 04

(e) Explain weighed codes. 04

(f) What is parity? How it can be used for error detecting? Explain with suitable example. 04

Q.2 a) Explain the operation of SR flip flop using NAND gates. What is a race around condition? 10

b) Design a 4 bit gray code to binary code converter using combinational logic design. 10

Q.3 a) Reduce using Quine McCluskey's method. 10

$F(A, B, C, D) = \pi M (2, 7, 8, 9, 10, 12)$

b) Design a full subtractor using logic gates. 07

c) What are the universal gates? And why they are used? 03

Q.4 a) Draw and explain the working of a binary asynchronous decade counter. 10

b) Implement $f(A, B, C, D) = M (1, 2, 3, 5, 6, 7, 8, 12, 13)$ using: 10

i) 8:1 MUX only one and a NOT gate

ii) 4:1 MUX only one and gates

Q.5 a) Compare various logic families. 10

b) Explain the operation of serial input serial output register. 10

Q.6 Write short notes on **any four** of the following: 20

(a) Counter ICs

(b) Hamming Code

(c) Excess-3 Code

(d) Parity Generator and Parity Checker Circuits

(e) Five and Six Variable K Maps
