

N.B.:

- 1) Question number 1 is compulsory arc compulsory.
- 2) Attempt any three questions from the remaining five questions.
- 3) Figures to the right indicate full marks.

- Q.1 Solve any five questions out of six questions.
- (a) Excess-3 code is called a self-completing code, Justify. [4]
 - (b) State and prove De-Morgan's theormos. [4]
 - (c) Simplify $y = \pi M(1,3,5)$ [4]
 - (d) Explain hazards in combinational circuits. [4]
 - (e) Explain race around condition? [4]
 - (f) Perform following operations using two's complement method:
i) $(42)_{10} - (18)_{10}$ ii) $(18)_{10} - (42)_{10}$ [4]
- Q.2 (a) Implement a full adder using 74138, 3:8 decoder. [10]
(b) Explain the operation of J-K Flip Flop using NAND gates. [10]
- Q.3 (a) Reduce using Quine McClusky's method: [10]
(b) Design a 4 bit binary code to gray code converter. [10]
- Q.4 (a) Obtain a 1:32 demultiplexer using four 1:8 demultiplexers and one 1:4 demultiplexer together. [10]
(b) Design a MOD 5 asynchronous UP counter using flip-flops. [10]
- Q.5 (a) Design a 2 bit magnitude comparator. [10]
(b) Design a BCD to seven segment converter with common cathode. [10]
- Q.6 Write short notes on any four of the following: [20]
(a) Shaft Position Encoding
(b) Describe both of the following:
i) Standard and Non-Standard SOP form ii) Standard and Non- Standard POS form
(c) Bidirectional shift register
(d) RTL and DTL Logic families
(e) Master-Slave Flip-Flop