MCA | Sem - I (IBSGS) / Computer Organisation & Architecture /

QP CODE : 514000 Nov-16

[Total Marks : 80

(3 Hours)

N.B. : 1) Question No.1 is **compulsory.**
2) Attempt any **four** from the remaining **six** questions.
3) Answer to sub-questions should be grouped together.

Q1. (a) Explain the construction and working of a DRAM with its circuit diagram. (07)

(b) Simplify the circuit represented by the given expression using a Karnaugh Map. Draw the original and the simplified circuit (07)

$$F(W,X,Y,Z)= \sum(0,1,2,4,5,6,8, 13) + d(12,13,15)$$

(c) Differentiate between RISC and CISC Processors. (06)

Q2. (a) What are Buses? Explain various methods for bus arbitration. (07)

(b) What is a De-Multiplexer? Construct a 1:8 De-Multiplexer using Logic Gates along with its truth table. Explain its working (08)

Q3. (a) Discuss various RAID levels in detail with suitable diagrams. (07)

(b) What is Cache memory? Explain various Cache mapping mechanisms. (08)

Q4. (a) Explain the concept of Six stage instruction pipelining? State its effect on conditional branching. (07)

(b) What are addressing modes? Explain different addressing modes with examples of each. (08)

Q5. (a) Explain the role of various General purpose registers and Control & Status registers in the CPU. (07)

(b) Discuss the functions of an I/O module. Explain Programmed I/O and Interrupt Driven I/O techniques. (08)

Q6. (a) Explain the construction and working of a Half adder with its truth table using logic gates. (07)

(b) Discuss various Instruction issue policies in Superscalar computers. (08)

Q7. Write Short Notes on **any three** :- (15)

a) NUMA
b) Instruction Cycle
c) DMA
d) D-Flip Flop
e) Interleaved Memory.
