(3 Hours) [Total marks: 80]

Note (1) Question No. 1 is compulsory.
(2) Attempt any three out of remaining five questions.
(3) Answer to sub-questions should be grouped together.

Q1.	(a)	Using K-Maps, simplify the following expression in four variables X, Y, Z, W. Draw logic diagram for the obtained solution. $F(X, Y, Z, W)=\Sigma(0,1,5,9,13,14,15)+d(3,4,7,10,11)$	5
	(b)	Explain the working of full adder with truth table and circuit diagram.	5
	(c)	Draw the instruction cycle state diagram indicating all of its sub cycles.	5
	(d)	Explain the role of MAR & MBR in instruction execution.	5
Q2.	(a)	Explain superscalar organization in brief. What are its limitations?	10
	(b)	What is I/O module? Explain all its function. Draw block diagram of I/O Module.	10
Q3.	(a)	Discuss 4 to 1 multiplexer & 1 to 4 de-multiplexer using truth table. Draw its implementation using the appropriate gates.	10
	(b)	Explain different types of parallel processing systems.	10
Q4.	(a)	Explain DMA technique in detail with the help of suitable diagram. Explain cycle stealing.	10
	(b)	Explain six stage instruction pipelines. How conditional branching affects pipeline performance?	10
Q5.	(a)	Define cache memory. Explain cache organization in detail.	10
	(b)	What are micro operations? Write micro operation for fetch cycle, interrupt cycle and indirect cycle.	10
Q6.		Write short note on <u>any four</u> of the following (a) JK Flip Flop (b) Register Renaming (c) SMP (d) Associative Memory (e) Interrupt driven I/O technique (f) Asynchronous counter	20

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