

Q. P. Code : 03674

(3 Hours)

Total Marks : 80

- N.B. :**
- 1) Question No.1 is **compulsory**.
 - 2) Attempt any **three** the remaining five questions.
 - 3) Answer to sub-questions should be grouped together.

1. (a) What is flipflop? Explain working of JK flipflop (05)
(b) Simplify the following expression using K-maps (05)
 $F(A,B,C,D) = \sum(1,7,10,13,14)+d(0,5,8,15)$
(c) Compare SRAM and DRAM (05)
(d) Explain principle and structure of cache memory (05)
2. (a) Explain bus interconnection structures. Explain bus arbitration? (10)
(b) Explain different addressing mode (10)
3. (a) Explain Programmed I/o, Interrupt I/O and DMA (10)
(b) Explain six stage instruction pipelining with suitable diagram (10)
4. (a) Explain superscalar organization and discuss the various superscalar instruction Issue Policies (10)
(b) What is RAID? Explain any three levels of RAID (10)
5. (a) Explain the different organization of multicore processors (10)
(b) List and explain the different addressing modes (10)
6. Write Short note on **(any four)** (20)
 - (a) Register Organization
 - (b) 1:4 Demultiplexer
 - (c) Flynn's classification
 - (d) Micro programmed and Hard wired control
 - (e) RISC and CISC architectures