MCA Sem I Choice BASED

Computer Orgn. & Architecture

19/5/2019 (32)

Q. P. Code : 03673

(3 Hours) Total Marks : 80

N.B. : 1) Question **No.1** is **compulsory.**
2) Attempt any three **four** from the remaining five questions.
3) Draw suitable diagrams wherever required.
4) Answers to sub-questions should be grouped together.

1. (a) Explain the role of the registers MAR and MBR in instruction execution. **(05)**
   (b) Construct a logic circuit using AND, OR and NOT gates. **(05)**
   $Y = \overline{(A + B)} \cdot (A + C) \cdot (B + C)$
   (c) Simplify the following expression using Karnaugh Maps **(05)**
   $F(A, B, C, D) = \sum m (1, 2, 7, 8, 10, 15) + d(3, 5)$
   (d) Explain the working of a DRAM. **(05)**

2. (a) What is cache memory? Explain the organisation of cache memories in detail. **(10)**
   (b) Discuss the role of a Bus in computer organisation. Explain various bus interconnection structures. **(10)**

3. (a) What are Flip Flops? How are they useful in digital circuits? Explain the construction and working of a J-K and D-Flip Flops with their truth tables. **(10)**
   (b) Discuss various factors that affect the design of an instruction in the instruction set of a processor. **(10)**

4. (a) Explain the structure and working of a Control Unit. **(10)**
   (b) What are interrupts? Explain methods for handling interrupts. **(10)**

5. (a) Explain the role of registers in a CPU. Discuss the organisation of registers in a CPU. **(10)**
   (b) Discuss various RAID levels with suitable diagrams. Explain advantages and disadvantages of each of them. **(10)**

6. Write Short Notes on **any four** of the following: **(20)**
   (a) Array Processors
   (b) Instruction Pipelining
   (c) Full Adder
   (d) De-multiplexer
   (e) Optical Memory.
