Q. P. Code: 27773

(3 Hours) [Total Marks : 80

N.B. : 1) Question **No.1** is **compulsory.**
2) Attempt any **three** from the remaining five questions.
3) Answers to sub-questions should be grouped together.

1. (a) Explain any two instruction addressing modes with suitable examples of each. (05)
   (b) Simplify the following Boolean expression using Karnaugh Map. (05)
   $F(A,B,C,D) = \sum(1,3, 8, 9, 11, 13, 14) + d(5, 6)$
   (c) Discuss the working of an Half adder with its truth table and circuit diagram. (05)
   (d) Explain the structure and working of an SRAM. (05)

2. (a) What are Multiplexers and de-multiplexers? Explain its use in logic circuits. Construct a 1:8 demultiplexer using basic logic gates and derive its truth table. (10)
   (b) Explain the role of registers in a CPU. Discuss the organisation of registers in a CPU. (10)

3. (a) What is a Control Unit? Explain the basic functions of a Control Unit. Discuss the basic model of a control unit along with its internal organization. (10)
   (b) Explain, how are multiple instructions executed by a processor. Discuss the six stage instruction pipelining mechanism with the help of a timing diagram. (10)

4. (a) Discuss the use of a Cache Memory. Explain various Cache mapping techniques. (10)
   (b) What are interrupts? Explain methods for handling interrupts. (10)

5. (a) Explain the basic organization of an I/O module with its block diagram. Discuss the Programmed I/O and Interrupt driven techniques for I/O operation. (10)
   (b) What is a RAID? Explain various RAID Levels in detail with the help of appropriate diagrams. (10)

6. Write Short Notes on **any four** of the following: (20)
   (a) Flynn's Taxonomy
   (b) R-S Flip Flop
   (c) Bus arbitration methods
   (d) RISC v/s CISC
   (e) Bus interconnections
   (f) NUMA