Q.P.Code: 37945

Max Marks: 80

Time: 3 Hours

N.B. 1) Question No.1 is compulsory
2) Solve any three questions from the remaining questions.
3) Assume suitable data if necessary.

1   Solve any four of the following.
(a) Explain behavior of gm as function of below parameters   5
     i.   Overdrive voltage with W/L constant.
     ii.   Overdrive voltage with ID constant.
(b) What are different second order effects in NMOS?   5
(c) Explain the concept of switched capacitor circuit   5
(d) Compare performance of various op-amp topologies   5
(e) Explain active current mirror circuit   5

2 (a) For W/L=50/0.5 and ID=0.5mA, calculate the transconductance and output   10
     impedance of both NMOS and PMOS device. Also find the intrinsic gain.
(b) What is a bandgap reference? Describe methods of implementation of band   10
     gap references.

3 (a) For common source stage with diode connected load, if the variation of $\acute{\eta}=$ 10
     gmb/gm with the output voltage is neglected. Prove that the gain is
     independent of bias current and voltages.
(b) Derive equation of differential gain, common mode gain and CMRR of   10
     differential amplifier.

4 (a) Explain the concept of clock feed through in charge pump. Charge injection,   10
     charge sharing in charge pump.
(b) Derive expression for voltage gain AV and output resistance Ro of source   10
     follower stage.

5   Design two stage operational amplifiers that meet the following specifications   20
     with a phase margin of 60. Assume the channel length is to be 1μm,
     K_N=100μA/V², K_P= 20μA/V², V_{TN} = |V_{TP}| = 0.5V, λ_N = 0.06V^{-1}, and λ_P =
     0.08V^{-1} Av>5000v/v, V_{dd}=2.5V, Vss= -2.5v, GB=5MHz, CL=10pf,
     SR>10v/μsec, Vout range=+/- 2V, ICMR= -1 to 2V, Pdiss≤ 2mw.

6   Write short note on any four
(a) Types of Noise of CS stage   5
(b) Cascode current mirror circuit.   5
(c) Advantage and disadvantages of DLL   5
(d) Comparison of full custom design and semi custom design   5
(e) Performance parameters of VCO   5

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