BE/Sem VII/CBSGS/ETRX/ICT/ND-17

Q.P. Code: 25912

Time: 3 Hours **Max Marks: 80**

N.B. 1) *Question No.1 is compulsory*
2) *Solve any three questions from the remaining questions.*
3) *Assume suitable data if necessary.*

Q.1.	Solve *any four* of the following	
(a)	What are the pros and cons of ion implantation vs diffusion?	5
(b)	Explain the difference between Dry Etching and Wet Etching	5
(c)	Explain High K and Low K dielectrics with application of each.	5
(d)	Explain difference between SOI Finfet and Bulk Finfet	5
(e)	Describe the SIMOX Method for fabrication of SOI	5
Q.2 (a)	Explain Czochralski method for silicon Crystal growth. What are its advantages?	10
Q.2(b)	Explain Interstitial and Substitutional diffusion process with example	5
Q.2(c)	Explain predeposition and drive in step in diffusion process	5
Q3.(a)	Explain the difference Between Positive Photo resist and Negative Photo resist.	5
Q.3(b)	Differentiate between Schottky contacts and Ohmic contacts	5
Q3 (c)	What is the significance of Design Rules? Draw layout for two input CMOS NOR gate using lambda (λ) based design rule.	10
Q.4(a)	What is LOCOS? Why it is required in CMOS Process. Explain technology solution for avoiding problems in LOCOS.	10
Q.4(b)	Develop the equations to describe the oxidation process (Deal-Grove Model).	10
Q.5(a)	Explain the fabrication Process steps along with vertical cross-sectional view for CMOS Inverter using N-well Process	10
Q.5(b)	With the help of a neat diagram describe Hayness-Schokly experiment for measurement of Drift Mobility of n-type semiconductor	10
Q.6	Write short notes on *any four* of the following. (a) The steps in Standard RCA cycle during wafer cleaning (b) Fabrication of MESFET (c) Electronics package reliability (d) Multigate device structures (e) Types of Thin Film Deposition	20

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