BE/ Sem VII / CBSGS / ETRX / ASIC Verification / M-J-18 04/06/18

Q.P. Code: 33595

Duration: 3 Hours Marks: 80

N. B. : (1) Question No. 1 is compulsory.
(2) Attempt any three out of remaining.
(3) Assume suitable data wherever required.

Q.1 Solve the following (Any four) 20 Marks

A. Differentiate between FPGA and CPLD.
B. Explain the necessity of randomization in system Verilog.
C. List the advantages of assertions in system Verilog.
D. What is DPI – C?
E. Explain the conditional coverage and branch coverage with suitable example.

Q.2 A. Discuss Silicon technology challenges. 10 Marks

B. Explain various data types in Verilog? Write Verilog code to swap contents of two registers with and without a temporary register? 10 Marks

Q.3 A. Explain the necessity and advantages of using interface. Elaborate with example. 10 Marks

B. Explain various types of arrays used in System Verilog. 10 Marks

Q.4 A. List the methods of interprocess communication. Explain any two in detail. 10 Marks

B. Describe immediate and concurrent assertions in detail. 10 Marks

Q.5 A. Draw and explain each block of Layered testbench used in verification. 10 Marks

B. What are different types of coverage? Explain line and toggle coverage with suitable example. 10 Marks

Q.6 A. Explain various Fork Join statements supported in System Verilog. 10 Marks

B. What is the significance of program block? For the interface, write the code for: 10 Marks

1. A clocking block that is sensitive to the negative edge of the clock and all I/O that are synchronous to the clock.
2. A modport for the testbench called master and a modport for the DUT called slave.
3. Use the clocking block in the I/O list for the master modport

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