B.E sem VII Rev.2012 CBSGS NID-2016 21-12-16

Sub:- ASIC Verification.

ETRX

Q. P. Code : 728901

Time:-3 Hrs **Marks: 80**

N.B. : 1. Question No. ONE is compulsory
2. Solve any THREE out of remaining questions
3. Assume suitable data if required

Q1. Solve the following (Any Four) **20 Marks**

A. Highlight the important features of Spartan -6 family devices.

B. What are semaphore and describe their use in SystemVerilog with suitable example.

C. Create a C function that prints out C: Hello World and Create a SystemVerilog module that calls the C function.

D. Describe the difference between code coverage and functional coverage. Which is more important and why we need them.

E. Enumerate the differences between rand and randc with suitable examples.

Q2. A. Give comparison of verification technology options. **05 Marks**

B. Create the SystemVerilog Code with the following requirements: **05 Marks**

I. Create a 512 location integer array
II. Create a 9-bit address variable to index into the array
III. Initialize the last location of the array to 5
IV. Call a task, my_task(), and pass it the array and the address
V. Create my_task() that takes two inputs, a constant 512-element integer array passed by reference, and a 9-bit address. The task calls a function, print_int(), and passes the array element, indexed by the address, to the function, pre-decrementing the address.
VI. Create print_int() that prints out the simulation time and the value of the input. The function has no return value.

C. Write the SystemVerilog code for the following items: **05 Marks**
1) Create a class ***Exercise1*** containing two variables, 8-bit *data* and 4-bit *address*. Create a constraint block that keeps *address* to 3 or 4.
2) In an *initial* block, construct an ***Exercise1*** object and randomize it. Check the status from randomization.

D. Explain the concept of switch level modeling and how it is done in verilog. Write switch level code for CMOS inverter in verilog. **05 Marks**

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Q3. A. What is necessity of clocking block and give detail explanation of clocking block with suitable example. **05 Marks**

B. Which are sequential control statements? Give one suitable example of each. **05 Marks**

C. Explain about the Timeunit, Timeprecision and timescale. **05 Marks**

D. What are different randomization built-in methods? Explain them with suitable examples. **05 Marks**

Q4. A. Explain various fork statements supported in systemverilog. **05 Marks**

B. With respect to SystemVerilog explain the following with suitable example **05 Marks**

I. Abstract classes

II. Parameterized classes

C. For the following code determine the order and time of execution for each statement if a join or join_none or join_any is used. The order and time of execution between the fork and join/join_none/join_ any is the same, only the order and execution time of the statements after the join are different. **05 Marks**

```
initial begin
  $display("@%0t: start fork...join_none example", $time);
  fork
        begin
          #20 $display("@%0t: sequential A after #20", $time);
          #20 $display("@%0t: sequential B after #20", $time);
        end
        $display("@%0t: parallel start", $time);
        #50 $display("@%0t: parallel after #50", $time);
        begin
          #30 $display("@%0t: sequential after #30", $time);
          #10 $display("@%0t: sequential after #10", $time);
        end
  join or join_any or join_none
  $display("@%0t: after join", $time);
  #80 $display("@%0t: finish after #80", $time);
end
```

D. Create a class called **MemTrans** that contains the following members, then construct a **MemTrans** object in an **initial** block **05 Marks**

i. An 8-bit **data_in** of logic type

ii. A 4-bit **address** of logic type

iii. A void function that **print** out the value of **data_in** and **address**

iv. Create a custom constructor, the **new** function, so that **data_in** and **address** are both initialized to 0.

[TURN OVER]

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Q5. A. For the code below, write a covergroup to collect coverage on the test plan requirement: "All ALU opcodes must be tested". Assume the opcodes are valid on the positive edge of signal ***clk***. **05 Marks**

```
typedef enum {ADD, SUB, MULT, DIV} opcode_e;

class Transaction;
  rand opcode_e opcode;
  rand byte operand1;
  rand byte operand2;
endclass
Transaction tr;
```

B. Where and how are assertions used? **05 Marks**

C. Explain how built-in method randomize() can be used as checker. **05 Marks**

D. Given the following code, determine what will be displayed. **05 Marks**

```
`default_nettype none
module test;
string students[$] = {"Amit", "Mohit", "Rohit"};
initial begin
  $display("Students[1] = %s", students[1]);
  students.insert(2, "Patil");
  $display("Students[2] = %s", students[2]);
  students.push_front("Ajay");
  $display("Students[2] = %s", students[2]);
  $display("pop_back = %s", students.pop_back);
  $display("students.size = %d", students.size);
end
endmodule // test
```

Q6. A. List and explain various coverage methods provided in SystemVerilog. **05 Marks**

B. Explain the following with suitable example **05 Marks**

a. Conditional coverage
b. Branch coverage

C. With suitable example for each, explain the following with respect to Sequences in assertions: **05 Marks**

a. Constant Range Delay
b. Nonconsecutive Repetition
c. Sequence And
d. Sequence Or
e. Sequence Within

D. Explain the layers of DPI-C. **05 Marks**

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