MAY – 2017

(20)

QP Code : 812901

(3 Hours) **[Total Marks : 80**

N. B. : (1) Question No. **1** is **compulsory**.
(2) Solve any **three** from remaining **five** questions.
(3) Draw neat labelled diagram wherever necessary.
(4) For layouts, use Graph paper.
(5) Assumptions should be clearly stated.

1. (a) State various data types in VHDL. **20**
(b) Explain flat band condition in MOS structure.
(c) Compare the effects of constant field and constant voltage scaling on power dissipation, current density and channel area.
(d) Explain latchup in CMOS.
(e) Draw the stick diagram for the two input :–
(i) CMOS NAND
(ii) Depletion load NMOS NOR

2. (a) Explain the structure of VHDL program. **5**
(b) Write a VHDL code for 4:1 mux. **5**
(c) Explain the twin tub process. **10**

3. (a) Calculate the threshold voltage V_{TO} at $V_{SB} = 0$ for a polysilicon gate n-channel MOS transistor with the following parameters, substrate doping density $N_A = 10^{16}$ cm^{-3}, polysilicon gate doping density $N_D = 2 \times 10^{20}$ cm^{-3}, $t_{ox} = 500^{o}$ A, $N_{ox} = 4 \times 10^{10}$ cm^{-2}, $\varepsilon_{si} = 11.7\ \varepsilon_0$ $\varepsilon_{ox} = 3.87\ \varepsilon_0$; $\varepsilon_0 = 8.854 \times 10^{-14}$ F/cm. **10**
(b) Explain the FPGA architecture. Explain the configuration logic blocks & I/O block of XC-4000 FPGA. **10**

4. (a) Explain the following processes used in fabrication :– **10**
(i) Photolithography
(ii) Epitaxy
(iii) Oxidation
(b) Draw the transfer characteristics of CMOS inverter and show clearly the transistor operating conditions under various regions of transfer curve. **6**
(c) Explain noise immunity & noise margin. **4**

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5. (a) Draw the stick diagram and λ based layout for 2 input NAND gate with depletion MOSFET as load with aspect ratio for the driver is 2:1 and load is 4:1. **10**

(b) State current - voltage relationship for, nMOS, pMOS transistors under various operating condition. **5**

(c) Explain the hot electron effect. **5**

6. Write short notes on the following :– **20**

(a) FET capacitances

(b) Features of VHDL

(c) stick diagram for $f = \overline{wx + y}$

(d) Buried contacts
