QP Code : 31401

(3 Hours)      [ Total Marks : 80

N. B. : (1) Question No. 1 is **compulsory**.
        (2) Attempt any **three** out of remaining **five**.
        (3) State your assumptions.

1. (a) Explain basic features of VHDL      5
   (b) Explain hot electron effect      5
   (c) Draw the voltage transfer characteristics of CMOS inverter and mark      5
       $V_{IH}$, $V_{OH}$, $V_{IL}$, $V_{OL}$
   (d) Explain oxidation, in VLSI fabrication      5

2. (a) Explain the twin tub process in detail      10
   (b) Explain latch-up in CMOS, and also explain methods to minimise      10

3. (a) Compare constant voltage and constant field scaling.      10
   (b) Write VHDL code for the following      10
       (i) 3:8 decoder
       (ii) Binary to gray code conversion

4. (a) Claculate the threshold voltage $V_{TO}$ at $V_{SB} = 0$ for a polysilicon gate      10
       n-channel MOS transistor with the following parameters
       $N_A = 10^{16}$ cm$^{-3}$ , $N_D = 2 \times 10^{20}$ cm$^{-3}$ , $t_{ox} = 500°A$
       $N_{OX} = 4 \times 10^{10}$ cm$^{-2}$ , $\varepsilon_{si} = 11.7 \, \varepsilon_0$; $\varepsilon_{OX} = 3.97 \times \varepsilon_0$;
       $\varepsilon_0 = 8.854 \times 10^{-14}$ F/cm
   (b) Compare MOS inverter with      10
       (i) Passive load
       (ii) E-nMOS as pull-up
       (iii) D-nMOS as pull-up
       (iv) CMOS inverter

5. (a) Implement the following function using NMOS & CMOS logic gates      10
      $F = \overline{x (yz + zw)}$
   (b) Explain the architecure of XC 4000 FPGA      10

6. Write short notes on following :—      20
   (a) Surface inversion condition in MOS structure
   (b) λ-based NMOS design rules
   (c) Buried and butt contacts
   (d) Lithography

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