

QP Code : 812902

(3 Hours)

[Total Marks : 80

- N. B. : (1) Question No. 1 is **compulsory**.
 (2) Solve any **three** from remaining **five** questions.
 (3) Draw neat labelled diagram wherever necessary.
 (4) For layouts, use Graph paper.
 (5) Assumptions should be clearly stated.

1. (a) Draw energy band diagram of NMOS structure and explain flat band condition indicating changes in the energy band diagram. 20
 (b) State the important features of VHDL.
 (c) Explain CVD process in VLSI fabrication.
 (d) Draw the transfer characteristics of CMOS inverter and define noise margins.

2. (a) Explain the architecture of FPGA XC 4000 with block diagrams/ 10
 (b) Write VHDL code for 4 bit full adder 10

3. (a) Find the threshold voltage of NMOS transistor having the substrate doping density $N_A = 10^{15}/\text{cm}^3$, the poly-gate doping density $N_D = 10^{20}/\text{cm}^3$, the gate oxide layer thickness $t_{\text{ox}} = 600 \text{ \AA}$, the fixed oxide charge $N_{\text{ox}} = 2 \times 10^{10}/\text{cm}^2$, the substrate bias voltage $V_{\text{SB}} = 2\text{V}$. Find V_T . 10
 (b) With neat diagram, explain n-well process of CMOS fabrication. 10

4. (a) (i) Write VHDL code for 2:4 decoder using process statement in behavioral style modelling. 5
 (ii) Write VHDL code for 1 bit full subtractor circuit. 5
 (b) (i) Explain voltage-current relationship of n-MOS transistor under various operating condition. 5
 (ii) Explain short channel effect in MOSFET. 5

5. (a) Derive relations of V_{IL} , V_{IH} , V_{OH} , V_{OL} for depletion load NMOS inverter in terms of device parameters. 10
 (b) Draw circuit diagram and stick diagram for the given expression 10
 $F = AB + AD$,
 (i) Using NMOS depletion load inverter circuit
 (ii) Using CMOS inverter

6. (a) Draw λ based layout for 2 input NAND gate with depletion MOSFET as load with aspect ratio for the driver is 2:1 and load is 4:1. 10
 (d) Distinguish between full scaling and constant voltage scaling. 10