B.E-VII Sem- Biomed

Very Large Scale Integrated Circuits.

(18) BE/VII/CBGS/BM/VLSIC

QP Code : **6009**

(3 Hours) [Total Marks :80

N.B. : (1) Question no. 1 is **compulsory.**
(2) Attempt any **three** questions from the remaining **five** questions.
(3) **Draw** a neat labelled diagram wherever **necessary.**
(4) **Assumptions** should be **clearly** stated.

1. (a) What are the different data types used in VHDL 5
(b) Write VHDL code for 2:4 decoder using process statement in behavioral style modelling. 5
(c) Explain surface inversion condition in MOS structure using band diagram. 5
(d) Explain latch up in CMOS circuits and ways to reduce it 5

2. (a) Draw the simplified block diagram of XC4000 series configurable logic blocks(CLB's) and explain briefly each subblocks. 10
(b) Write VHDL code for 4 bit full adder. 10

3. (a) Explain briefly the different modeling techniques used in VHDL. 5
(b) Differentiate between constant voltage and constant field scaling used in VLSI 7
(c) Draw circuit diagram, stick diagram and layout using λ-based design rule for 2-input CMOS NOR gate. use proper colour coding 8

4. (a) Calculate the threshold voltage at room temperature for $V_{SB} = 0$ for a PMOS transistor fabricated on n-type substrate with bulk doping density of $N_D = 10^{16}/cm^3$, gate doping density (n-type poly) of $N_D = 10^{20}/cm^3$, $Q_{ox} = q \times 4 \times 10^{10}/cm^2$ and oxide thickness $t_{ox} = 0.1\mu m; \epsilon_{si} = 11.7 \times \epsilon_0, \epsilon_{ox} = 3.97 \times \epsilon_0$ $\epsilon_0 = 8.85 \times 10^{-14} F/cm$. $T = 30^0 C$. 7
(b) Explain different MOS capacitance in detail 5
(c) Draw stick diagram and layout of 2-input NAND gate using n-MOS depletion load. aspect ratio for the drivers is 2:1 and load is 4:1 8

5. (a) Explain the twin tub process of fabrication of CMOS inverter in detail. 10
(b) Explain-wafer processing, oxidation and photo lithograhy used in semi conductor fabrication technology in detail. 10

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6. (a) Draw the circuit diagram of CMOS inverter and explain various regions of operation of the transistors based on the transfer characteristics. 10

(b) Calculate the noise margins of the the following depletion-load inverter circuit. 10

$V_{DD} = 5.0V$

$V_{TO,driver} = 1.0V \quad V_{TO,load} = -3.0V$

$(W/L)_{driver} = 2, (W/L)_{load} = 1/3$

$k'_{n,driver} = k'_{n,load} = 25\mu A/V^2$

$\lambda = 0.4V^{1/2}$, where λ is body effect coefficient/substrate coefficient

$\phi_F = -0.3V$