Time: 3 Hours **Marks: 80**

N.B.: (1) Question No. 1 is Compulsory.

(2) Attempt any three questions out of the remaining five.

(3) Each question carries 20 marks and sub-question carry equal marks.

(4) Assume suitable data if required.

1. **Attempt any FOUR** (20)

a) Define Preemptive and non preemptive scheduling.

b) Compare Deadlock avoidance and deadlock prevention.

c) Define terms Speedup, Efficiency, Throughput related to pipeline

d) Why is there a need for communication between two processes? Also write technique to implement IPC.

e) Draw and explain a typical Instruction Cycle in a processor.

2 (a) Explain Flynn's Classification in details. (10)

(b) Explain Pre-emptive scheduling. And Find out Average waiting Time (AWT) and Average Turn around Time (TAT) for the following. (10)

Jobs	Burst Time	Arrival Time
J1	4	0
J2	1	1
J3	2	2
J4	1	3

3 (a) Explain FIFO page replacement algorithm. Find out Miss Ratio, Hit ratio for the Following string using FIFO method.

(Consider page frame size = 3)

2, 3, 2, 1, 5, 2, 4, 5, 3, 2, 5, 2 (10)

(b) Explain various pipeline hazards. Explain the performance metrics for instruction Pipelines.

4. (a) Explain FCFS scheduling. For the given FCFS scheduling, calculate the average waiting time and average turnaround time. (10)

Process Id	Arrival Time	Burst Time
P1	0	8
P2	1	4
P3	2	9
P4	3	5

(b) Describe the register organization within the CPU . (10)

5. (a) Explain Multi core Architecture in details . (10)

(b) Explain in detail Hardwired control unit. Discuss any one method to implement it. (10)

6. Write a short note on (20)

a) Cluster
b) Superscalar Architecture
c) File Organization and Access
d) Virtual Memory

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